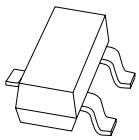


PESD5V0S2BT

Low capacitance bidirectional double ESD protection diode

Rev. 03 — 9 February 2009 Product data sheet

1. Product profile

1.1 General description

Low capacitance bidirectional double ElectroStatic Discharge (ESD) protection diode in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package designed to protect two data lines from the damage caused by ESD and other transients.

1.2 Features

- Bidirectional ESD protection of two lines
- Low diode capacitance
- Max. peak pulse power: P_{PP} = 130 W at t_p = 8/20 µs
- Low clamping voltage: V_{CL} = 14 V at I_{PP} = 12 A
- Ultra low leakage current: I_{RM} = 5 nA at V_{RWM} = 5 V
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PP} = 12 A at t_p = 8/20 µs

1.3 Applications

- Cellular handsets and accessories
- Portable electronics
- Computers and peripherals
- Communication systems
- Audio and video equipment

1.4 Quick reference data

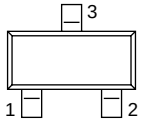
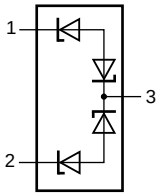
Table 1. Quick reference data

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	-	35	45	pF

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode 1		
2	cathode 2		
3	double cathode		

sym031

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0S2BT	-	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking

Type number	Marking code[1]
PESD5V0S2BT	*G5

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per diode						
P_{PP}	peak pulse power	t_p = 8/20 µs	[1][2]	-	130	W
I_{PP}	peak pulse current	t_p = 8/20 µs	[1][2]	-	12	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform.

[2] Measured from pin 1 to 3 or pin 2 to 3.

Table 6. ESD maximum ratings

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	-	30	kV
		MIL-STD-883 (human body model)		-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 to 3 or pin 2 to 3.

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

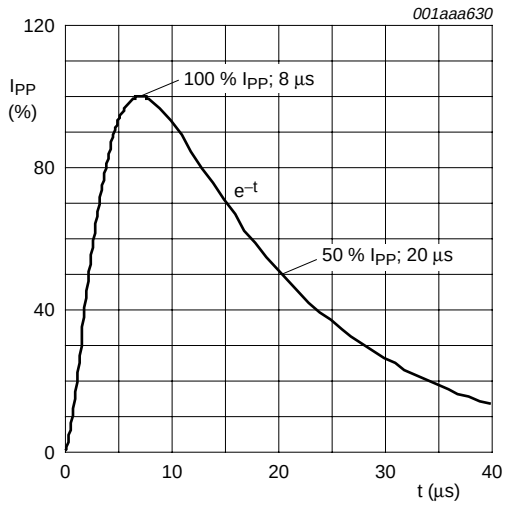


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

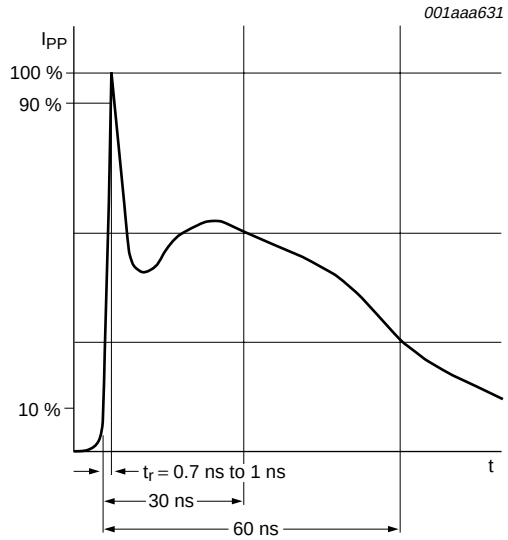


Fig 2. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

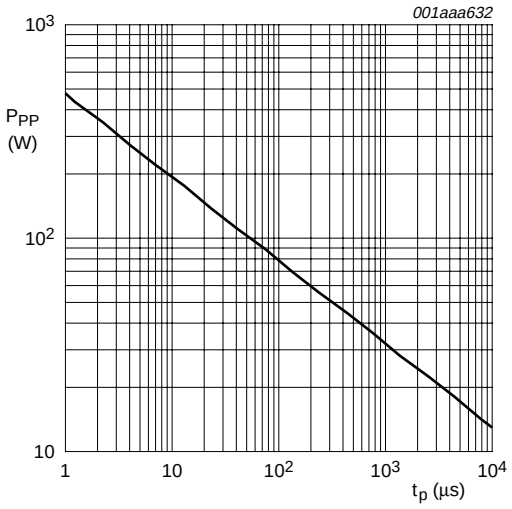
Table 8. Electrical characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
V_{RWM}	reverse standoff voltage			-	-	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V		-	5	100	nA
V_{CL}	clamping voltage	I_{PP} = 1 A	[1][2]	-	-	10	V
		I_{PP} = 12 A	[1][2]	-	-	14	V
V_{BR}	breakdown voltage	I_R = 1 mA		5.5	-	9.5	V
r_{dif}	differential resistance	I_R = 1 mA		-	-	50	Ω
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	35	45	pF

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform.

[2] Measured from pin 1 to 3 or pin 2 to 3.



T_{amb} = 25 °C

t_p = 8/20 µs exponential decay waveform

Fig 3. Peak pulse power dissipation as a function of pulse duration; typical values

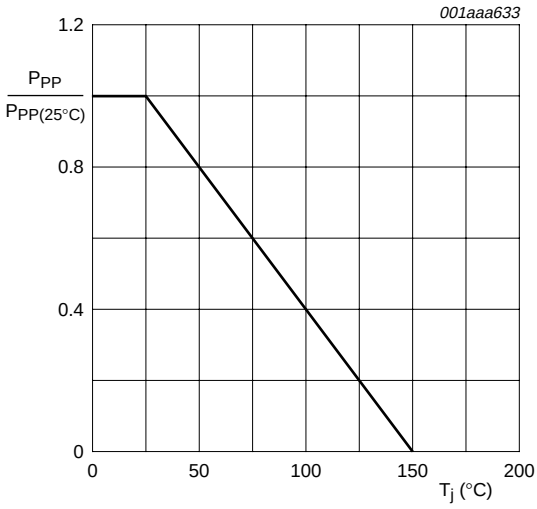
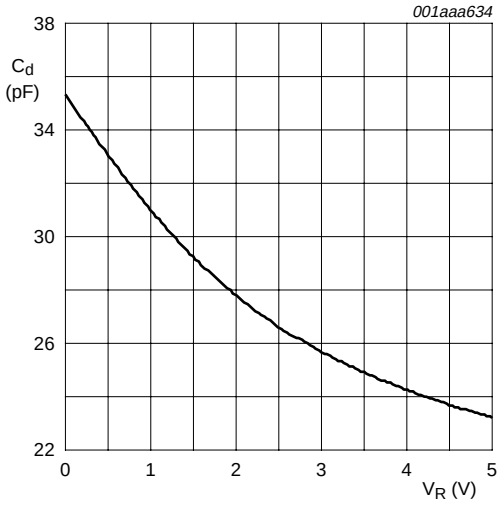
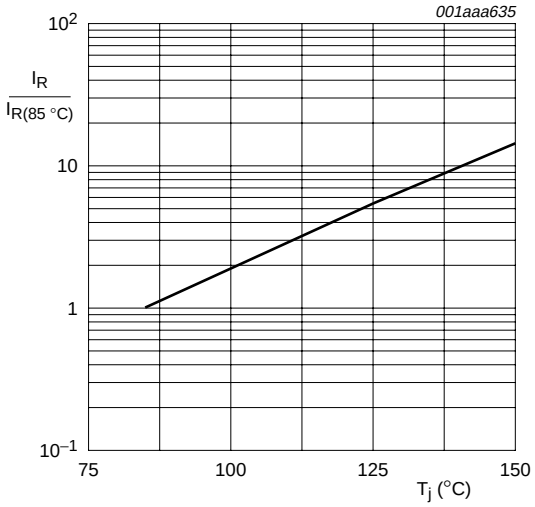


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values



T_{amb} = 25 °C; f = 1 MHz

Fig 5. Diode capacitance as a function of reverse voltage; typical values



I_R < 1 nA measured at T_{amb} = 25 °C

Fig 6. Relative variation of reverse current as a function of junction temperature; typical values

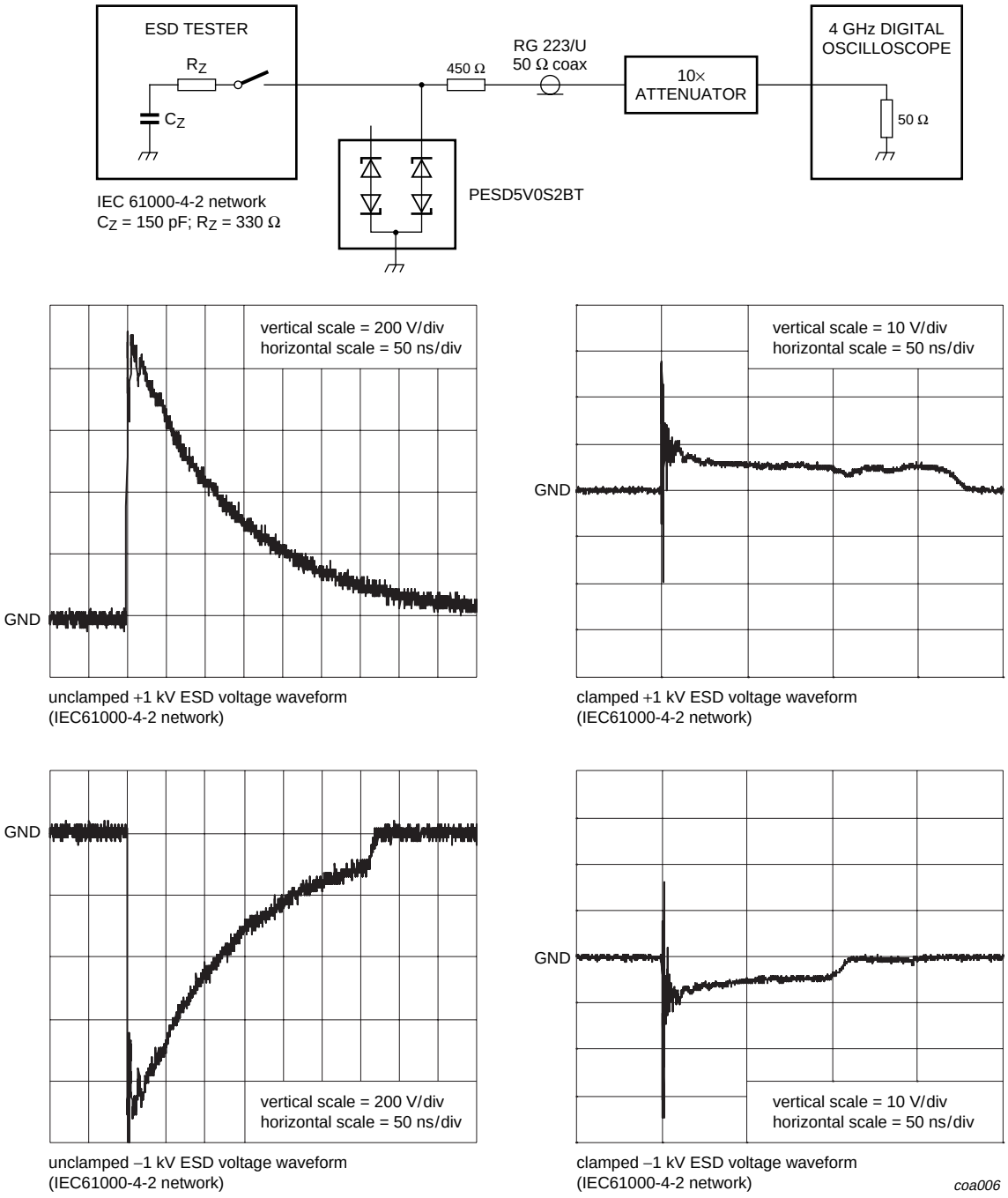


Fig 7. ESD clamping test setup and waveforms

7. Application information

The PESD5V0S2BT is designed for the bidirectional protection of two lines from the damage caused by ElectroStatic Discharge (ESD) and surge pulses.
The PESD5V0S2BT may be used on lines where the signal polarities are both, positive and negative with respect to ground. The PESD5V0S2BT provides a surge capability of 130 W per line for an 8/20 µs waveform.

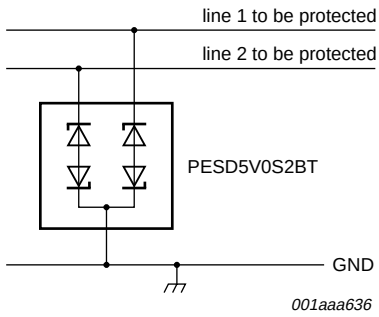


Fig 8. Typical application for bidirectional protection of two lines

Circuit board layout and protection device placement:

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESD5V0S2BT as close to the input terminal or connector as possible.
2. The path length between the PESD5V0S2BT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

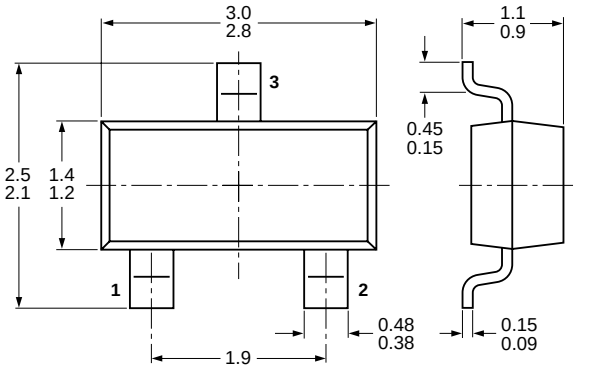


Fig 9. Package outline SOT23 (TO-236AB)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PESD5V0S2BT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235

[1] For further information and the availability of packing methods, see Section 13.

10. Soldering

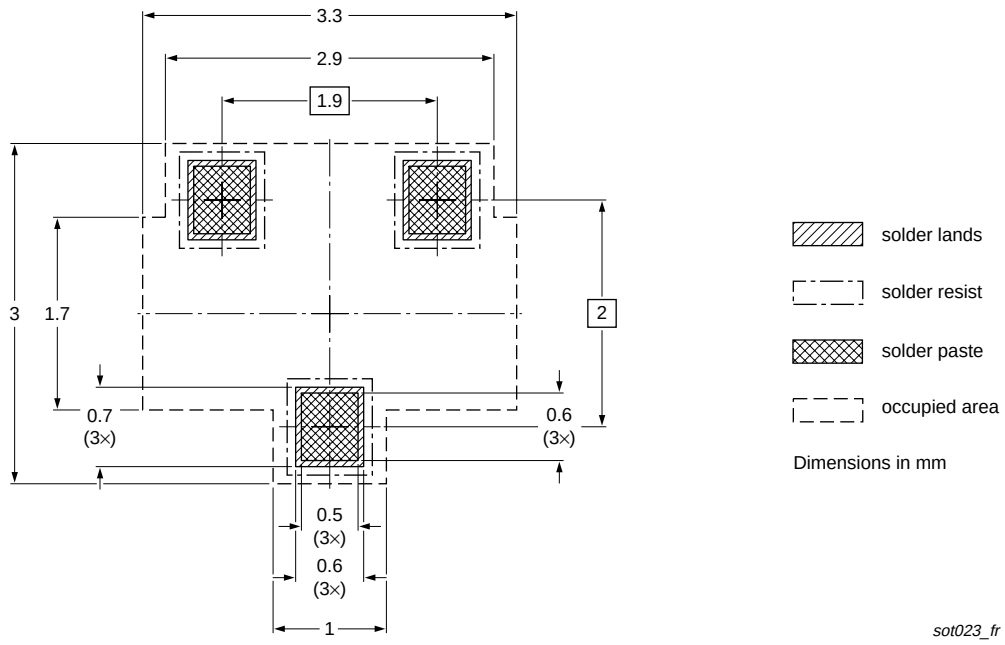


Fig 10. Reflow soldering footprint SOT23 (TO-236AB)

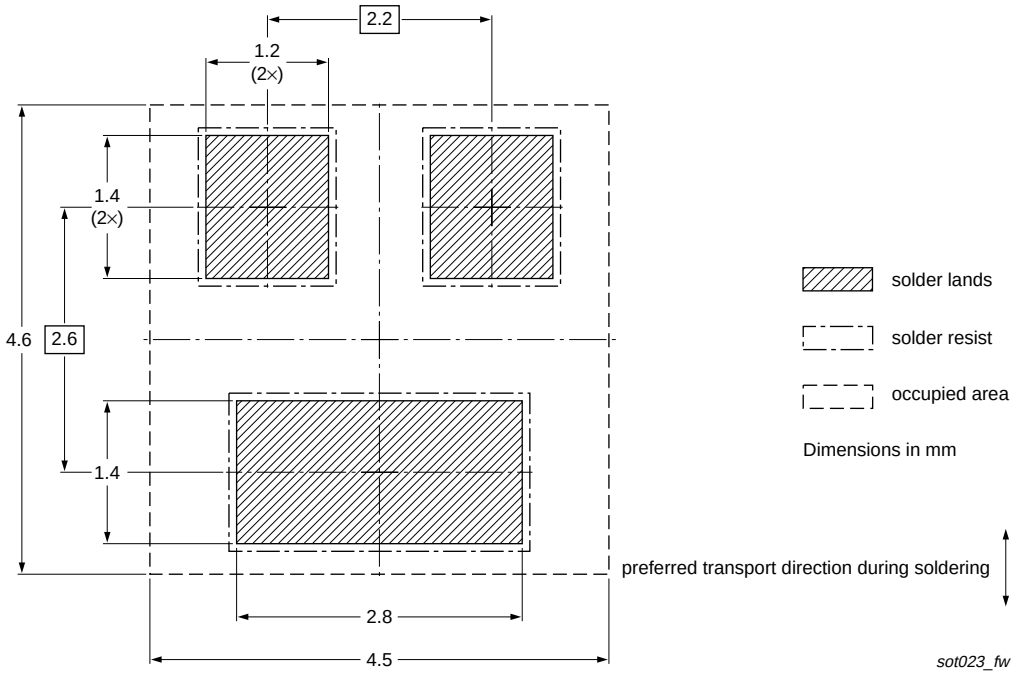


Fig 11. Wave soldering footprint SOT23 (TO-236AB)

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0S2BT_3	20090209	Product data sheet	-	PESD5V0S2BT_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6: ESD electro static discharge capability redefined to V_{ESD} electrostatic discharge voltage • Table 8: $V_{(CL)R}$ clamping voltage redefined to V_{CL} • Figure 4: figure notes removed • Section 7 “Application information”: updated • Figure 9: superseded by minimized package outline drawing • Section 9 “Packing information”: added • Section 10 “Soldering”: added • Section 12 “Legal information”: updated			
PESD5V0S2BT_2	20040527	Product data sheet	-	PESD5V0S2BT_1
PESD5V0S2BT_1	20040517	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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